Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**115”**

**SOURCE**

**G**

**144”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .021 x .021” min.**

**Backside Potential: DRAIN**

**Mask Ref: GEN 5.5**

**APPROVED BY: DK DIE SIZE .115” X .144” DATE: 11/15/21**

**MFG: INT’L RECTIFIER THICKNESS .010” P/N: IRFC240NB**

**DG 10.1.2**

#### Rev B, 7/1